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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,665	03/20/2006	Robert Linley Muir	17497US01	4619

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	PAPER NUMBER
2115	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,665	MUIR, ROBERT LINLEY	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-17,19-28 and 30-35* is/are rejected.

7)☒ Claim(s) *7,18 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/16/06, 12/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 3/30/06

2. Claims 1-34 are pending for examination.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 8/16/06, 12/26/06 were considered by the examiner.

Claim Objections

5. Claim 6 objected to because of the following informalities: Spelling "Cryptrographic". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5-6, 8-11, 13-14, 16-17, 19-27-28, 30-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Davis et al. U.S. Patent No. 6,401,208 ("Davis").

8. As per claim 1, Davis discloses a processing system comprising:

a central processor [110];

a BIOS memory device [170] storing a boot program;

a BIOS protection device [130];

a plurality of memory address and data paths [160] to provide communication between at least the processor, BIOS memory device and BIOS protection device; said BIOS protection device configured to verify the boot program and control the memory address and data paths and prevent execution of the boot program [625-645 – insertion of wait states] until said verification [fig. 6A, 6B].

9. As per claim 2, Davis discloses the BIOS protection device is in communication between a central processor and the BIOS memory device [fig. 1], the BIOS protection device configured to include address and data path interface connections, and an authentication processor, the BIOS protection device configured to control the address and data path to which it is connected and the authentication processor configured to interrogate the BIOS memory device connected to the address and data path to determined if the boot program contained in the BIOS memory device is authentic, and if the boot program is determined to be authentic permit execution of the boot program [col. 5 lines 33-54, 61-65, col. 6 lines 20-27].

10. As per claim 3, Davis discloses the address and data path interfaces are selected from a group comprising a serial interface, a totally non-multiplexed bus, an intel LPC bus structure [col. 5 lines 1-3].

11. As per claim 5, Davis discloses the BIOS memory device includes a cryptographic structure located at a know location in the BIOS memory device [181-182].

12. As per claim 6, Davis discloses the BIOS protection device cryptographic structure is a digital signature [182] and the BIOS protection device is configured to calculate the value of the cryptographic structure from contents of the BIOS memory device and an internal public key and interrogates the BIOS memory device to verify that the correct cryptographic structure is present and corresponds with the boot program, or a part thereof stored in the BIOS memory device [fig. 6B – col. 4 lines 40-59].

13. As per claim 8, Davis discloses the central processor, the BIOS memory device and the BIOS protection device are mounted on a mother board [fig. 1] configured to be inoperative if the BIOS protection device is not present [inherent].

14. As per claim 9, Davis discloses a reset control circuit is provided in the BIOS protection device such that the mother board cannot exit the reset state if the BIOS protection device is not present [inherent as show in col. 6 lines 20-27].

15. As per claim 10, Davis discloses the BIOS protection device will hold the reset signal in the reset state while the authentication of the BIOS is performed [col. 7 lines 44-65].

16. As per claim 11, Davis discloses when the authentication is successful, the BIOS protection device releases the reset signal allowing the central processor to commence operation [col. 6 lines 20-27].

17. As per claim 12, Davis discloses the BIOS protection device inserts wait cycles to disable the central processor while authenticating the BIOS memory device [col. 5 line 32].

18. As per claim 35, Davis discloses a processing system comprising a processor [110] connected to a BIOS memory device containing a boot program [170] through a connection path, the BIOS protection device forms part of the connection path [fig. 1 – connection path from 110 to 170], the BIOS protection device operable to check the authenticity of the boot program and allow the processor to execute the boot program only if the check of the boot program indicates that it is authentic [fig. 6A, 6B].

19. Claims 1, 13, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Helbig, Sr. U.S. Patent No. 6,564,326.

20. As per claim 1, Helbig, Sr. discloses a processing system comprising:

a central processor [24];

a BIOS memory device [col. 4 lines 20-26] storing a boot program;

a BIOS protection device [10];

a plurality of memory address and data paths to provide communication between at least the processor, BIOS memory device and BIOS protection device; said BIOS protection device configured to verify the boot program and control the memory address and data paths and prevent execution of the boot program until said verification [col. 4 lines 27-35; claim 30].

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. Claims 1, 13, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hannah U.S. Patent No. 6,735,696.

24. As per claim 1, Hannah teaches a processing system comprising:

a central processor [50];

a BIOS memory device [60] storing a boot program;

a BIOS protection device [58];

a plurality of memory address and data paths [Local Bus 52] to provide communication between at least the processor, BIOS memory device and BIOS protection device; said BIOS protection device configured to verify the boot program and prevent execution of the boot program until said verification [col. 4 line 62 to col. 5 line 5; claim 7].

Hannah does not explicitly teach the BIOS protection device takes control of the address and data paths.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to include the take control of the memory address and data paths. One of ordinary skill in the art would have expected applicant's invention to perform equally well with either the claimed taking control of memory address and data paths to prevent execution of the boot program until verification or to verify the boot program before it is permitted control of the processor taught by Hannah because they both perform the same function of protecting the system from invalid BIOS boot code.

Therefore, it would have been an obvious matter of design choice to modify Hannah to obtain he invention as specified in claim 1.

Allowable Subject Matter

25. Claims 7, 18, 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Examiner's note:

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran

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